Confirmation No. 3317

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	DETECHEVERRY	Examiner:	Baisa, Joselito
Serial No.:	10/564,582	Group Art Unit:	2832
Filed:	January 12, 2006	Docket No.:	NL030878US (NXPS.267PA)
Title:	INDUCTIVE AND CAPACITIVE ELEMENTS FOR SEMICONDUCTOR TECHNOLOGIES WITH MINIMUM PATTERN DENSITY REQUIREMENTS		

APPEAL BRIEF

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P.O. Box 1450
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Customer No.
65913

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed October 15, 2009 and in response to the rejections of claims 1-22 as set forth in the Final Office Action dated July 22, 2009.

Please charge Deposit Account number 50-4019 (NL030878US) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-22 stand rejected and are presented for appeal. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated July 22, 2009.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

The claimed invention, in certain embodiments, is directed to an important advancement involving the use of tilling structures in a semiconductor device that includes an inductor. Appellant's tilling structures are electrically connected together and arranged in

a geometrical pattern that substantially inhibits an inducement of an image current in the tilling structures that is caused by a current in the inductor. Appellant recognized that using tilling structures with specific geometrical arrangements relative to the inductor prevents the inducement of an image current in the tilling structures and thus enabling the use of such tilling structures in a device with an inductor. *See, e.g.,* Appellant's Figures 3-5 and 7-9. Tilling structures (as is known in the art) are used to increase or decrease the pattern density in empty or large metal areas, respectively, of a semiconductor device. *See, e.g.,* page 1:21-28 of Appellant's Specification and U.S. Patent No. 7,152,215, Col. 1:54-59. Tilling structures improve manufacturability of the semiconductor device, for example, by improving planarity, by improving the integrity of dielectric material, and/or by improving the uniformity of the removal rate of Chemical Mechanical Polishing. In the discussion below, the claims are directed to semiconductor devices that include an inductor and tilling structures.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a semiconductor device comprising a plurality of layers (*see, e.g.*, device 10 shown in Figs. 1 and 2, and page 8:5-19). The semiconductor device includes a substrate (*see, e.g.*, substrate 20 shown in Fig. 2, and page 8:14-15) having a first major surface and an inductive element (*see, e.g.*, element 11 shown in Fig. 1, and page 8:6-7) fabricated on the first major surface of the substrate the inductive element comprising at least one conductive line. The semiconductor device further includes a plurality of tilling structures in at least one layer (*see, e.g.*, metal stripes 12 and pattern 14 shown in Fig. 1, and page 8:10-12), the plurality of tilling structures arranged to improve manufacturability of the semiconductor device (*see, e.g.*, page 1:21-29), wherein the plurality of tilling structures are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element (*see, e.g.*, page 8:16 to page 9:11).

Commensurate with independent claim 22, an example embodiment of the present invention is directed to a method for providing an inductive element in a semiconductor device comprising a plurality of layers (*see, e.g.*, device 10 shown in Figs. 1 and 2, and page 8:5-19). The method includes providing a substrate having a first major surface (*see, e.g.*,

substrate 20 shown in Fig. 2, and page 8:14-15), forming an inductive element (*see, e.g.*, element 11 shown in Fig. 1, and page 8:6-7) above the first major surface of the substrate, the inductive element comprising at least one conductive line, providing a plurality of tilling structures (*see, e.g.*, metal stripes 12 and pattern 14 shown in Fig. 1, and page 8:10-12) in at least one layer to improve manufacturability of the semiconductor device (*see, e.g.*, page 1:21-29), wherein the plurality of tilling structures are electrically connected together and are arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element (*see, e.g.*, page 8:16 to page 9:11).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1-3, 5-7, 9 and 11-22 stand rejected under 35 U.S.C. § 103(a) over Ballantine (U.S. Patent No. 6,489,663) in view of Minami (U.S. Patent No. 6,730,983).

B. Claims 4, 8 and 10 stand rejected under 35 U.S.C. § 103(a) over the '663 reference in view of the '983 reference and further in view of Kuroda (U.S. Patent No. 6,693,315).

VII. Argument

A. The § 103(a) Rejection Of Claims 1-3, 5-7, 9 And 11-22 Is Improper Because The Cited Combination Of References Does Not Correspond To The Claimed Invention And The '663 Reference Teaches Away From The Proposed Combination.

1. The § 103(a) Rejection Of Claims 1-3, 5-7, 9 And 11-22 Is Improper Because The Cited References Fail To Disclose Tilling Structures Arranged In A Geometrical Pattern To Substantially Inhibit The Inducement Of An Image Current In The Tilling Structures.

The cited references do not teach a plurality of tilling structures that are arranged in a geometrical pattern so as to substantially inhibit the inducement of an image current in the

tilling structures by a current in an inductive element as claimed, and the Examiner's attempt to assert such teachings in the references is erroneous. The claimed invention, in certain embodiments, is directed to an important advancement that enables tilling structures to be used in a semiconductor device that includes an inductor. Appellant recognized that using tilling structures with specific geometrical arrangements relative to the inductor prevents the inducement of an image current in the tilling structures that is caused by current flowing through the inductor. As a result, Appellant's tilling structures can be used in semiconductor devices that include an inductor thereby improving manufacturability of such semiconductor devices. *See, e.g.,* Appellant's Figures 3-5 and 7-9 and page 1:21-28 of Appellant's Specification. The cited references, however, do not teach tilling structures that are arranged to inhibit the inducement of an image current in the tilling structures, and nothing in the record supports the Examiner's assertions regarding the alleged operation of unrelated structures in the cited references. As such, the § 103 rejection necessarily fails.

More specifically, the '663 reference does not teach that vias 28 (*i.e.,* the asserted tilling structures) are arranged to substantially inhibit the inducement of an image current in the vias 28 by a current in inductor 16 (*i.e.,* the asserted inductive element). Instead, the '663 reference arranges the vias 28 to terminate the electric field lines emanating from inductor 16 and to decrease the parasitic capacitance present between inductor 16 and ground strips 26. *See, e.g.,* Figure 1 and Col. 5:40-45. Appellant notes that the only discussion in the '663 reference relating to preventing the flow of an image current is directed to preventing the flow of an image current in the ground strips 26 (*see, e.g.,* Col. 3:38-41, Col. 4:39-42 and Col. 6:59-62). Thus, the '663 reference does not teach arranging the vias 28 to prevent the flow of an image current in the vias 28.

In a failed attempt to address the '633 reference's lack of correspondence, the Examiner erroneously asserts that the '663 reference's configuration of ground strips 26 and vias 28 "will inhibit the inducement of an image current from an inductive element. The current is directed to the grounding strip [Col. 6, Lines 59-64]." *See* page 8 of the Final Office Action. The relied upon portion of the '663 reference (*i.e.,* Col. 6:59-64) does not mention current being directed to the ground strips, but instead teaches preventing the flow of an image current in the ground strips. Appellant notes that the Examiner appears to be

asserting that current is being directed from the vias 28 to the ground strips 26. As such, the Examiner illogically attempts to rely upon current being induced in the vias 28 to somehow assert that the vias 28 are arranged to inhibit inducement of an image current in the vias 28. The Examiner has not presented any evidence of record (from the '663 reference or otherwise) to support the assertion that the vias 28 are arranged in the manner of the claimed invention. Thus, the Examiner's assertion regarding the alleged teachings of the '663 reference is mere speculation that is unsupported by the evidence of record and upon which it is improper to base a rejection. As discussed above, the '663 reference does not teach arranging the vias 28 to prevent the flow of an image current in the vias 28. Appellant notes that the '983 reference is not alleged by the Examiner and in fact does not address the above discussed deficiencies of the primary '663 reference. For example, the '983 reference does not teach or suggest that dummy elements 12 are arranged to prevent the inducement of an image current in the dummy elements 12. Because none of the cited references teach preventing the inducement of an image current in tilling structures, no reasonable combination of these references can provide correspondence to the claimed invention.

In view of the above, the § 103(a) rejection of claims 1-3, 5-7, 9 and 11-22 is improper and Appellant requests that it be reversed.

2. The § 103(a) Rejection Of Claims 1-3, 5-7, 9 And 11-22 Is Improper Because The '663 Reference Teaches Away From The Proposed Combination.

The '663 reference teaches away from the Examiner's proposed combination which would undermine the purpose of the '663 reference. Consistent with the recent *KSR* decision, M.P.E.P. § 2143.01 explains the long-standing principle that a §103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('663) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (U.S. 2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.").

Turning now to the impropriety of the Examiner's proposed combination, the modification of the '663 reference would apparently result in vias 28 being electrically

connected to substrate 12 (*see* Figure 1 of the '663 reference) since dummy elements 12 of the '983 reference are electrically connected to substrate 1 (*see* Figure 2 of the '983 reference). Modifying the vias 28 as asserted would result in high frequency-energy passing through the vias 28 into substrate 12 (as taught by the '983 reference at Col. 2:26-28), thereby increasing coupling between the substrate 12 and the inductor 16 relative to the unmodified vias 28 of the '663 reference. However, the inductor 16 and vias 28 are to be isolated from the substrate 12 (*see, e.g.,* Figure 1 and Col. 4:52-64 of the '663 reference). Thus, the Examiner's proposed modification of the '663 reference would render the '663 reference unsatisfactory for its intended purpose of preventing coupling between the substrate 12 and the inductor 16 (*e.g.,* by preventing the electric field lines generated by the inductor from penetrating into the substrate). *See, e.g.,* Col. 3:62-67. Accordingly, the '663 reference teaches away from the Examiner's proposed modification and there would be no motivation for the skilled artisan to modify the '663 reference in such a manner.

Appellant further notes that the Examiner has failed to address the previously-explained impropriety of the Examiner's proposed combination of the '663 and '983 references, in Appellant's traversals of record, as required, for example, by M.P.E.P. § 707.07(f). As such, the record stands uncontested with regard to the impropriety of the Examiner's proposed combination of the '663 and '983 references, and the § 103(a) rejections must be reversed.

In view of the above, the § 103(a) rejection of claims 1-3, 5-7, 9 and 11-22 is improper and Appellant requests that it be reversed.

3. The § 103(a) Rejection Of Claims 6 And 7 Is Improper Because The Cited References Fail To Disclose Tilling Structures That Do Not Block Penetration Into The Substrate Of Electric Field Lines Generated By An Inductor.

The cited references do not teach a geometrical pattern of tilling structures that does not substantially inhibit inductive coupling between the inductive element and the substrate (*see* claim 6). The cited references also do not teach that a geometrical pattern of tilling structures that does not substantially block penetration into the substrate of electric field lines generated by the inductive element (*see* claim 7). In short, the Examiner improperly bases

the rejection of claim 6 and 7 on assertions regarding the alleged teachings of the '663 reference that are directly contradicted by the '663 reference.

More specifically, the Examiner's assertion that the '663 reference's vias 28 (*i.e.*, the asserted tilling structures) do not block the penetration of electric field lines from inductor 16 to substrate 12 (and do not substantially inhibit inductive coupling between inductor 16 to substrate 12) are directly contradicted by the '663 reference which states that the orientation of the vias 28 "effectively places conducting vias 28 in a position to intercept and terminate the electric field emanating from spiral inductor 16." Col. 5:14-16. The Examiner's further reliance upon ground plane 22 (prior art Figure 4 of the '663 reference) is wholly improper because the '663 reference expressly teaches that the disclosed arrangement of ground strips 26 and vias 28 replaces ground plane 22, with the disclosed arrangement performing the function of the ground plane (*e.g.*, to block the electric field emanating from the inductor and to inhibit inductive coupling between the inductor and the substrate). *See, e.g.*, Figure 1 and Col. 6:56-67. Thus, the '663 reference expressly teaches that the vias 28 block the penetration of electric field lines from inductor 16 to substrate 12.

In view of the above, the § 103(a) rejection of claims 6 and 7 is improper and Appellant requests that it be reversed.

4. The § 103(a) Rejection Of Claims 17-19 Is Improper Because The Cited References Fail To Disclose A Device That Includes An Inductive Element, Tilling Structures And A Capacitive Element.

The Examiner's proposed combination of the cited references does not teach a device having a capacitive element as in the claimed invention. In particular, the cited portions of the '663 reference do not teach that vias 28 (*i.e.*, the asserted tilling structures) form one electrode of a capacitive element and that ground strips 26 (*i.e.*, the asserted ground shield) form another electrode of the capacitive element as in claims 17 and 19. Instead, the '663 reference teaches that the vias 28 decrease the parasitic capacitance present between inductor 16 and ground strips 26. *See, e.g.*, Figure 1 and Col. 5:40-45.

Moreover, the '663 reference expressly states that "In the preferred embodiment shown, the conducting vias are shown terminating between and slightly below the wires of the inductor because that is the configuration that most effectively keeps the capacitance

down." Col. 4:65 to Col. 5:1. Thus, the '663 reference uses vias 28 to prevent the IC 200 from functioning as a capacitor between inductor 16 and ground strips 26. Appellant notes that the Examiner's failed attempt to maintain the rejection apparently relies upon asserting that ground strips 26 form one electrode of the capacitor and that inductor 16 forms the other electrode of the capacitor. *See* page 9 of the Final Office Action ("Each of the vias 28 or grounding strip 26 forms an electrode of a capacitive element with the conductive element of inductor 16."). As such, the Examiner has acknowledged that there is no correspondence to the claimed invention which requires that the tilling structures form one electrode and the ground shield forms the other electrode. The claimed inductive element does not form one of the electrodes of the capacitive element as asserted by the Examiner's alleged correspondence. Accordingly, the Examiner's proposed combination does not correspond to the claimed invention.

In view of the above, the § 103(a) rejection of claims 17-19 is improper and Appellant requests that it be reversed.

B. The § 103(a) Rejection Of Claims 4, 8 and 10 Is Improper Because The Cited Combination Of References Does Not Correspond To The Claimed Invention And Because The '663 Reference Teaches Away From The Proposed Combination.

The § 103 rejection of claims 4, 8 and 10 is improper because the cited combination of the '663 and '983 references does not correspond to the claimed invention as discussed above under heading A(1). Moreover, the '663 reference teaches away from the Examiner's proposed combination as discussed above under heading A(2). Appellant notes that the '315 references is not alleged by the Examiner to address the above discussed deficiencies of the cited combination of the '663 and'983 reference. For at least these reasons, the § 103 rejection of claims 4, 8 and 10 is improper since these claims depend from claim 1.

In view of the above, Appellant requests that the § 103 rejection of claim 4, 8 and 10 be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-22 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

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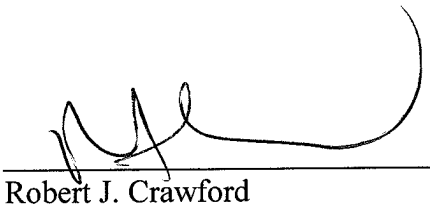
By: 

Robert J. Crawford
Reg. No.: 32,122
Eric J. Curtin
651-686-6633
(NXPS.267PA)

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/564,582)

1. A semiconductor device comprising a plurality of layers, the semiconductor device comprising:

a substrate having a first major surface,

an inductive element fabricated on the first major surface of the substrate the inductive element comprising at least one conductive line,

a plurality of tilling structures in at least one layer, the plurality of tilling structures arranged to improve manufacturability of the semiconductor device,

wherein the plurality of tilling structures are electrically connected together and arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element.

2. A semiconductor device according to claim 1, the tilling structures being made from tilling structure material, wherein the plurality of tilling structures are arranged in a pattern so that the amount of tilling structure material in an area closer to the inductive element is smaller than the amount of tilling structure material in an area farther away from the inductive element.

3. A semiconductor device according to claim 1, wherein the tilling structures are located at different layers, tilling structures at each layer being arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element, and wherein the arrangement of the tilling structures is determined by a desired pattern density of the semiconductor device for improving at least one of a process window of lithography, uniformity of Chemical Mechanical Polishing removal rate and integrity of low-k dielectrics.

4. A semiconductor device according to claim 3, wherein the geometrical pattern of tilling structures at two different layers is different in shape and/or orientation.

5. A semiconductor device according to claim 3, wherein the tilling structures at different layers are electrically connected to each other.

6. A semiconductor device according to claim 1, wherein the geometrical pattern of tilling structures does not substantially inhibit inductive coupling between the inductive element and the substrate, and wherein the tilling structures are connected to a DC potential.

7. A semiconductor device according to claim 1, wherein the geometrical pattern of tilling structures does not substantially block penetration into the substrate of electric field lines generated by the inductive element, and wherein the tilling structures are a plurality of slender elongate elements.

8. A semiconductor device according to claim 1, wherein the tilling structures are a plurality of substantially triangular elements.

9. A semiconductor device according to claim 7, wherein the elements of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element.

10. A semiconductor device according to claim 8, wherein the elements of the tilling structures are locally oriented perpendicular to the at least one conductive line of the inductive element.

11. A semiconductor device according to claim 1, furthermore comprising a ground shield for shielding the inductive element from a further layer.

12. A semiconductor device according to claim 11, wherein the further layer is the substrate.

13. A semiconductor device according to claim 11, furthermore comprising connection means electrically connecting the plurality of tilling structures with the ground shield without creating a conductive loop.

14. A semiconductor device according to claim 1, wherein the tilling structures are formed in a region other than a region directly below the inductive element.

15. A semiconductor device according to claim 1, furthermore provided with a further passive element.

16. A semiconductor device according to claim 15, wherein the further passive element is a capacitive element.

17. A semiconductor device according to claim 16, wherein the capacitive element comprises two capacitor electrodes at least one of the capacitor electrodes being formed by a plurality of tilling structures.

18. A semiconductor device according to claim 17, wherein a capacitor electrode formed by a plurality of tilling structures leads to a metal or polysilicon or active region density in the inductor vicinity respecting the design rules of advanced IC technologies.

19. A semiconductor device according to claim 17, wherein one capacitor electrode of the capacitive element is formed by a ground shield.

20. A semiconductor device according to claim 16, wherein the integration of the capacitive element with the inductive element is optimized to respect the metal pattern density in advanced silicon technologies.

21. A semiconductor device according to claim 16, wherein the distance between the capacitive element and the inductive element is large enough to avoid a dominant fringe coupling between them.

22. A method for providing an inductive element in a semiconductor device comprising a plurality of layers, the method comprising:

providing a substrate having a first major surface,

forming an inductive element above the first major surface of the substrate, the inductive element comprising at least one conductive line,

providing a plurality of tilling structures in at least one layer to improve manufacturability of the semiconductor device,

wherein the plurality of tilling structures are electrically connected together and are arranged in a geometrical pattern so as to substantially inhibit an inducement of an image current in the tilling structures by a current in the inductive element.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.